


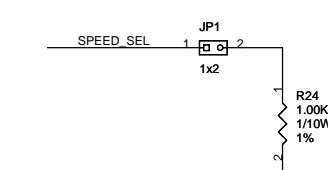
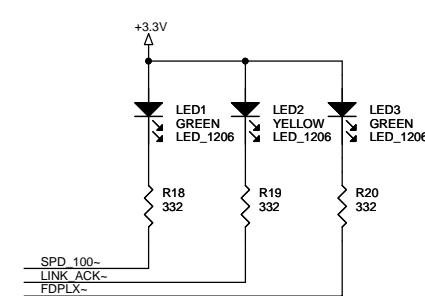
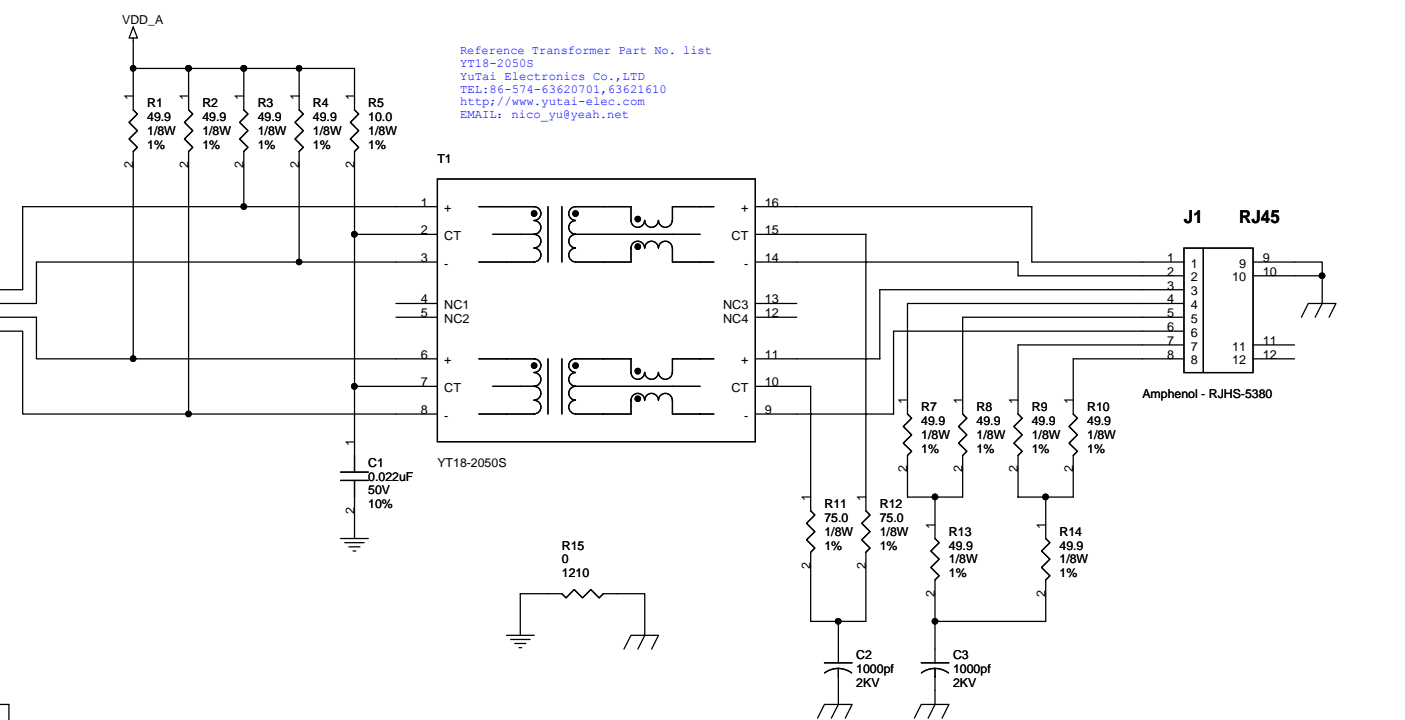
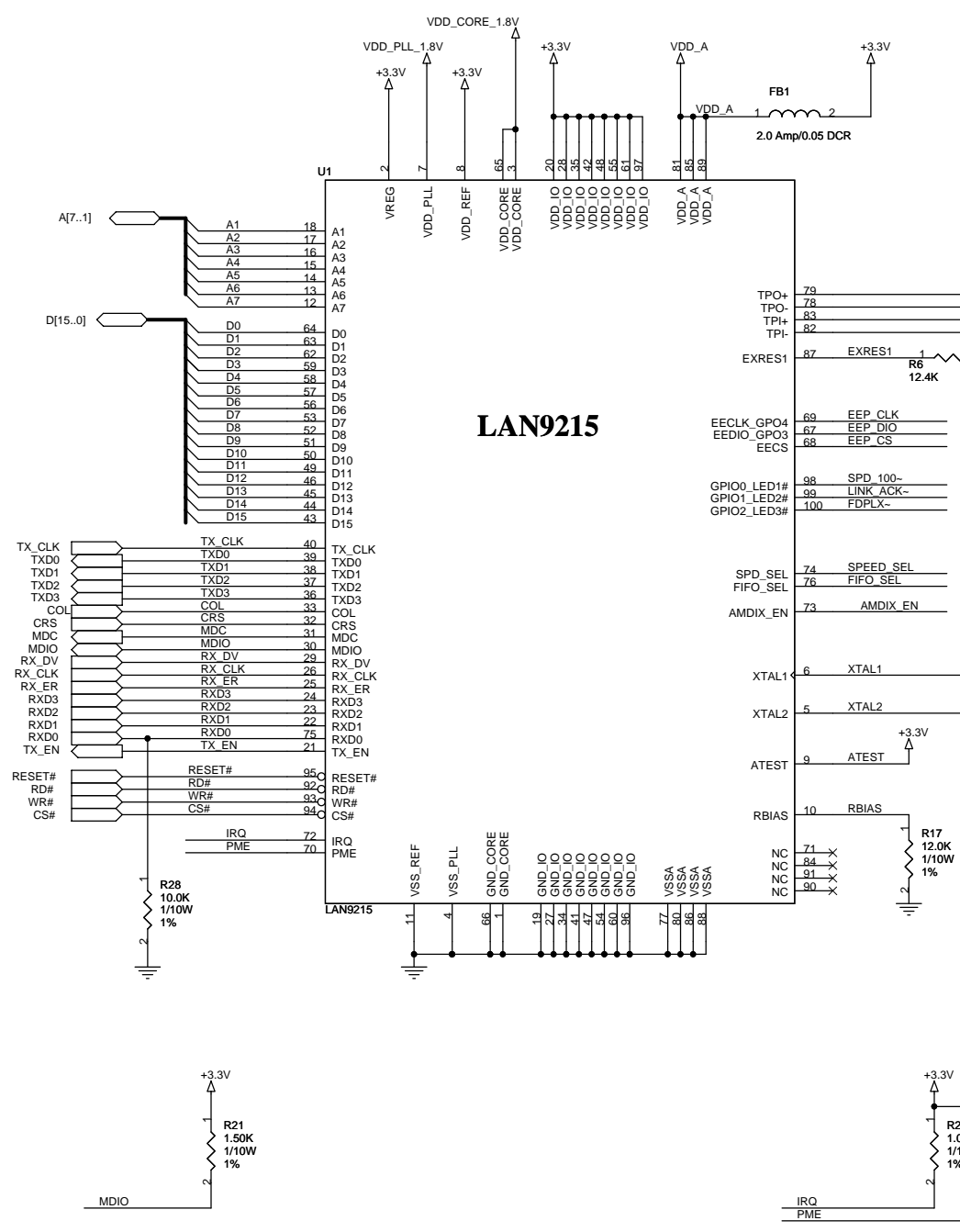
# LAN9215 Reference Schematic

Schematic Revision 0.5

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Circuit diagrams utilizing SMSC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMSC or others. SMSC reserves the right to make changes at any time in order to improve design and supply the best product possible.

			
Title <b>LAN9215 Reference Schematic</b>			
Size C	Engineer N/A	Assembly No. N/A	Rev 0.5
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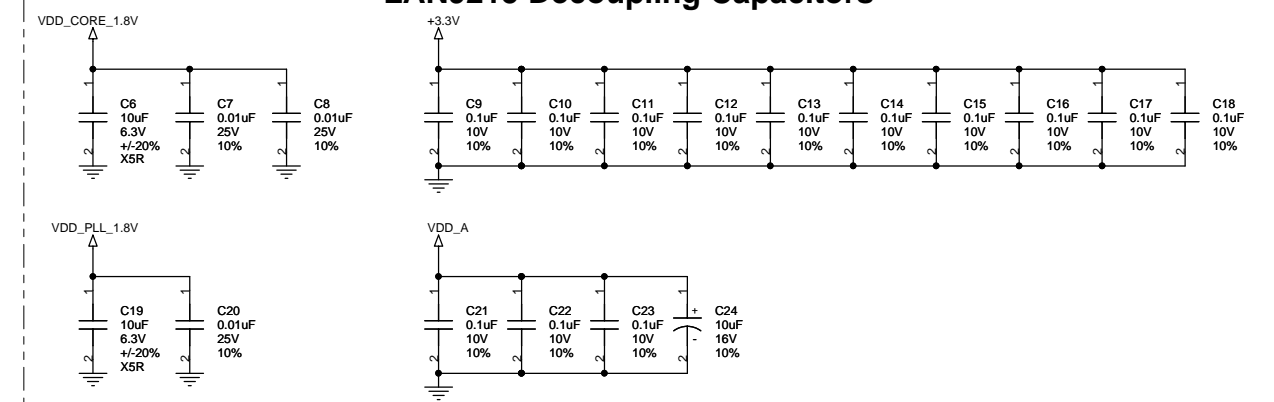


NOTE:  
 FIFO\_SEL can be driven dynamically and is not pulled internally to either state. This pin has the same timing as the Address Bus and can be driven by upper address bits not used by the LAN9215. Refer to datasheet.

NOTE:  
 IN = 10Mbps, Half-Duplex, Auto Neg. Disabled  
 OUT = 100Mbps, Half-Duplex, Auto Neg. Enabled

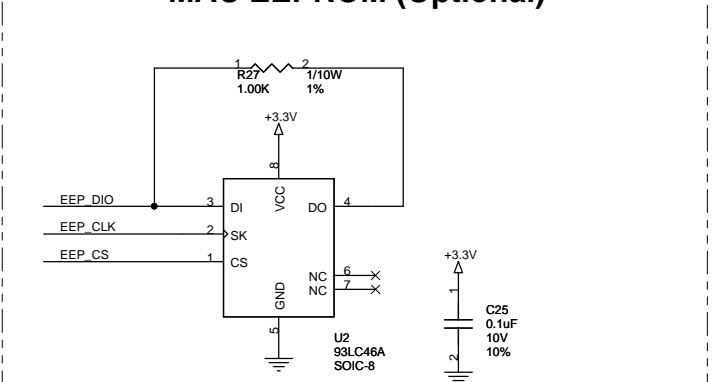
NOTE:  
 IN = Auto-MDIX Functionality Enabled  
 OUT = Auto-MDIX Functionality Disabled

### LAN9215 Decoupling Capacitors



NOTE:  
 C6 and C19 must be low ESR capacitors. Ceramic is recommended.

### MAC EEPROM (Optional)



**SMSC**  
 SUCCESS BY DESIGN

Title: **LAN9215 Reference Schematic**

Size	Engineer	Assembly No.	Rev
C	N/A	N/A	0.5

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